AMENDMENT TO THE CLAIMS

1. (Currently amended) An electrically alterable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region with a first channel region defined therebetween, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer;

a first floating gate ~~having a first height and~~ comprising a conductive material, the first floating gate being disposed adjacent the first diffusion region and above the first channel region, separated therefrom by a first insulator region, the first floating gate being capable of storing electrical charge injected into the first floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate relative to the first diffusion region;

a second floating gate ~~having a second height and~~ comprising a conductive material, the second floating gate being disposed adjacent the second diffusion region

and above the first channel region, separated therefrom by a second insulator region, the second floating gate being capable of storing electrical charge injected into the second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate relative to the second diffusion region; and

a control gate ~~having a third height higher than both the first height and the second height and~~ comprising a conductive material, the control gate being disposed laterally between the first floating gate and the second floating gate, the control gate being separated from the first floating gate by a first vertical insulator layer and being separated from the second floating gate by a second vertical insulator layer, such that the first and second floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate acting as a word select line, the control gate further being disposed above the first channel region without overlapping the two spaced-apart diffusion regions, being separated therefrom by a third insulator region;

wherein the first dopant has P-type characteristics.

2-3. (Canceled)

4. (Previously presented) The memory device of claim 1, wherein the first insulator region has a thickness that allows tunneling of charge between the first floating gate and the first channel region.

5. (Original) The memory device of claim 4, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

6. (Previously presented) The memory device of claim 1, wherein the second insulator region has a thickness that allows tunneling of charge between the second floating gate and the first channel region.

7. (Previously presented) The memory device of claim 6, wherein the thickness of the second insulator region is between 70 Angstroms and 110 Angstroms.

8. (Previously presented) The memory device of claim 1, wherein the first vertical insulator is made from a silicon dioxide having a thickness that provides capacitance between the first floating gate and the control gate, and wherein the first vertical insulator prevents leakage between the first floating gate and the control gate.

9. (Previously presented) The memory device of claim 1, wherein the first vertical insulator is made from an oxide-nitride-oxide layer having a thickness that provides a capacitance between the first floating gate and the control gate, and wherein the first vertical insulator prevents leakage between the first floating gate and the control gate.

10. (Previously presented) The memory device of claim 1, wherein the second vertical insulator is made from a silicon dioxide having a thickness that provides a capacitance between the second floating gate and the control gate, and wherein the second vertical insulator prevents leakage between the second floating gate and the control gate.

11. (Previously presented) The memory device of claim 1, wherein the second vertical insulator is made from an oxide-nitride-oxide layer having a thickness that provides a capacitance between the second floating gate and the control gate, and wherein the second vertical insulator prevents leakage between the second floating gate and the control gate.

12-14. (canceled)

15. (Previously presented) The memory device of claim 1, wherein the first floating gate and the second floating gate are each capable of storing multiple levels of charge.

16. (Previously presented) The memory device of claim 1, wherein the first floating gate and the second floating gate are each capable of storing four levels of charge.

17. (Original) The memory device of claim 1, wherein an oxidation layer is disposed on top of each diffusion region.

18-40. (canceled)

41. (Currently amended) An electrically alterable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, with a first channel region defined therebetween, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer;

a first floating gate having a left side, and a right side and comprising a conductive material, the first floating gate being disposed adjacent the first diffusion region and above the first channel region and being separated therefrom by a first insulator region, the first floating gate being capable of storing electrical charge injected into the first floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate relative to the first diffusion region;

a second floating gate having a left side, and a right side and comprising a conductive material, the second floating gate being disposed adjacent the second diffusion region and above the first channel region, being separated therefrom by a second insulator region, the second floating gate being capable of storing electrical charge injected into the second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate relative to the second diffusion region; and

a control gate comprising a conductive material, the control gate being disposed laterally between the first floating gate and the second floating gate, the control gate being separated from the first floating gate by a third insulator layer and being separated from the second floating gate by a fourth insulator layer, such that the first and second floating gates are each capacitively coupled to have an electrical potential derived from the electrical potential of the control gate,the control gate covering the first floating gate on at least right side and left side, the control gate further covering the second floating gate on at least right side and left side, the control gate further being disposed above the first channel region and separated therefrom by a third insulator region;

wherein the first dopant has P-type characteristics.

42-43. (Canceled)

44. (Previously presented) The memory device of claim 41, wherein the first insulator region has a thickness that allows tunneling of charge between the first floating gate and the first channel region.

45. (Previously presented) The memory device of claim 44, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

46. (Previously presented) The memory device of claim 41, wherein the second insulator region has a thickness that allows tunneling of charge between the second floating gate and the first channel region.

47. (Previously presented) The memory device of claim 46, wherein the thickness of the second insulator region is between 70 Angstroms and 110 Angstroms.

48. (Previously presented) The memory device of claim 41, wherein the third insulator is made from a silicon dioxide layer having a thickness that provides a capacitance between the first floating gate and the control gate, and wherein the third insulator prevents leakage between the first floating gate and the control gate.

49. (Previously presented) The memory device of claim 41, wherein the third insulator is made from an oxide-nitride-oxide layer having a thickness that provides a capacitance between the first floating gate and the control gate, and wherein the third insulator prevents leakage between the first floating gate and the control gate.

50. (Previously presented) The memory device of claim 41, wherein the fourth

insulator is made from a silicon dioxide layer having a thickness that provides a capacitance between the second floating gate and the control gate, and wherein the fourth insulator ~~preventing~~ prevents leakage between the second floating gate and the control gate.

51. (Previously presented) The memory device of claim 41, wherein the fourth insulator is made from an oxide-nitride-oxide having a thickness that provides a capacitance between the second floating gate and the control gate, and wherein the fourth insulator ~~preventing~~ prevents leakage between the second floating gate and the control gate.

52. (Previously presented) The memory device of claim 41, wherein the first floating gate and the second floating gate are each capable of storing multiple levels of charge.

53. (Previously presented) The memory device of claim 41, wherein the first floating gate and the second floating gate are each capable of storing four levels of charge.

54. (Previously presented) The memory device of claim 41, wherein an oxidation layer is disposed on top of each diffusion region.

55. (Currently amended) An electrically alterable memory device, comprising:

a first semiconductor layer doped with a first dopant in a first concentration;

a second semiconductor layer, adjacent the first semiconductor layer, doped with a second dopant that has an opposite electrical characteristic than the first dopant, the second semiconductor layer having a top side;

two spaced-apart diffusion regions embedded in the top side of the second semiconductor layer, each diffusion region being doped with the first dopant in a

second concentration greater than the first concentration, the two diffusion regions including a first diffusion region and a second diffusion region, with a first channel region defined therebetween ~~the first diffusion region and the second diffusion region~~, wherein the second semiconductor layer and each diffusion region form a junction which is capable of a soft avalanche breakdown in response to a lower electrical potential imposed on the diffusion region relative to the second semiconductor layer;

a first floating gate comprising a conductive material, the first floating gate being disposed adjacent the first diffusion region and above the first channel region and being separated therefrom by a first insulator region, the first floating gate being capable of storing electrical charge injected into the first floating gate in response to the soft avalanche breakdown and a higher electrical potential at the first floating gate relative to the first diffusion region;

a second floating gate comprising a conductive material, the second floating gate being disposed adjacent the second diffusion region and above the first channel region, being separated therefrom by a second insulator region, the second floating gate being capable of storing electrical charge injected into the second floating gate in response to the soft avalanche breakdown and a higher electrical potential at the second floating gate relative to the second diffusion region; and

a control gate having at least two lateral sides and comprising a conductive material, the control gate being disposed laterally between the first floating gate and the second floating gate, the control gate being separated from the first floating gate by a first vertical insulator layer and being separated from the second floating gate by a second vertical insulator layer, such that the first and second floating gates are each

capacitively coupled to have an electrical potential derived from the electrical potential of the control gate, the control gate being covered by the first floating gate on more than one lateral side and being covered by the second floating gate on more than one lateral side, the control gate being separated from the first channel region by a third insulator region;

wherein the first dopant has P-type characteristics.

56-57. (Canceled)

58. (Previously presented) The memory device of claim 55, wherein the first insulator region has a thickness that allows tunneling of charge between the first floating gate and the first channel region.

59. (Previously presented) The memory device of claim 58, wherein the thickness of the first insulator region is between 70 Angstroms and 110 Angstroms.

60. (Previously presented) The memory device of claim 55, wherein the second insulator region has a thickness that allows tunneling of charge between the second floating gate and the first channel region.

61. (Previously presented) The memory device of claim 55, wherein the thickness of the second insulator region is between 70 Angstroms and 110 Angstroms.

62. (Previously presented) The memory device of claim 55, wherein the first vertical insulator is made from a silicon dioxide layer having a thickness that provides a capacitance between the first floating gate and the control gate, and wherein the first vertical insulator prevents leakage between the first floating gate and the control gate.

63. (Previously presented) The memory device of claim 55, wherein the first vertical insulator is made from an oxide-nitride-oxide having a thickness that provides a capacitance between the first floating gate and the control gate, and wherein the first vertical insulator prevents leakage between the first floating gate and the control gate.

64. (Previously presented) The memory device of claim 55, wherein the second vertical insulator is made from a silicon dioxide layer having a thickness that provides a capacitance between the second floating gate and the control gate, and wherein the second vertical insulator prevents leakage between the second floating gate and the control gate.

65. (Previously presented) The memory device of claim 55, wherein the second vertical insulator is made from an oxide-nitride-oxide layer having a thickness that provides a capacitance between the second floating gate and the control gate, and wherein the second vertical insulator prevents leakage between the second floating gate and the control gate.

66. (Previously presented) The memory device of claim 55, wherein the first floating gate and the second floating gate are each capable of storing multiple levels of charge.

67. (Previously presented) The memory device of claim 55, wherein the first floating gate and the second floating gate are each capable of storing four levels of charge.

68. (Previously presented) The memory device of claim 55, wherein an oxidation layer is disposed on top of each diffusion region.